

Keeping pace with technology

How synchronous
memory (SDRAM)
will impact top-level
IS planning.

Quarterly information for CIOs

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Some things never change,
but then again...



For almost 10 years

DRAM architecture has remained

stable and memory upgrades easy to implement.

As a top level IS person, memory wasn't something

you needed to spend much time thinking about.

Well, all of that is about to change, and change

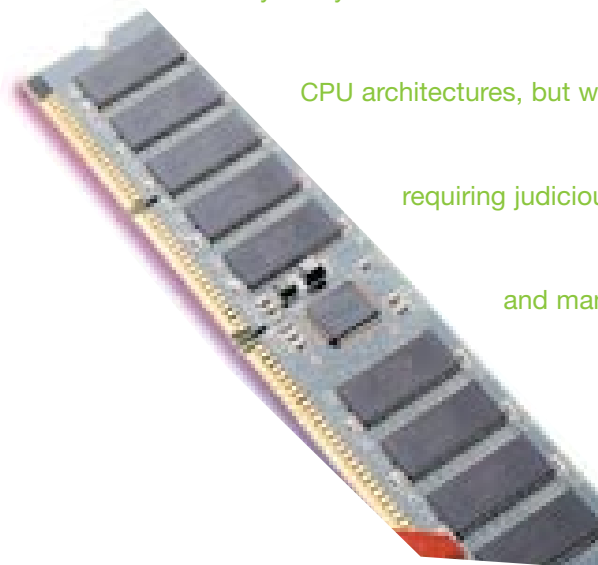
quickly. The shifts we are talking about will enable

your systems to take advantage of new bus and

CPU architectures, but will come at a cost,

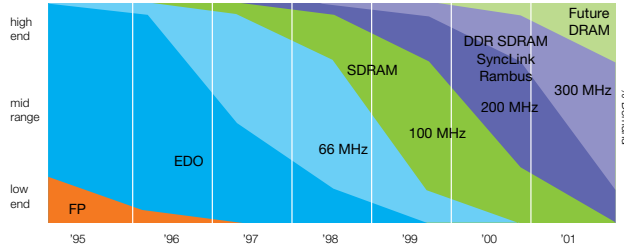
requiring judicious on-going planning

and management.



DRAM end-use conversion

Source: Samsung



Getting in sync

Synchronous DRAM, introduced earlier this year, is the first real shift in core memory design since the late 1980s. The performance criteria for SDRAM, while only subtly different from today's asynchronous standard DRAM, will make a world of difference in how memory is viewed in overall system performance and lifecycle management.

Users expect their systems to nimbly handle all types of streamed data. Bus traffic flows across the PCI bus between DRAM, SCSI devices, IDE, ISA, USB and soon Firewire-based peripherals. These data streams include network traffic, video, and high-fidelity audio inputs from digital-video disk (DVD) and hard disk subsystems.

Move over processor

For the last decade the CPU has been the driving element in overall system performance. Today, as we move to specialized

subsystems, a balanced system will determine the ultimate system performance. As new systems emerge, CPUs are packed with ever-greater resources, but the fear is that current memory architectures would not be able to keep pace with the steady stream of instructions from the memory to the processor. Multiple resource demands on the CPU mean a single cache miss can domino into the halt of several instructions and cause unstable delivery of streamed data. In addition, new engines such as graphics accelerators, I/O servers and multimedia processors live on the same system bus as the SDRAM and each can concurrently demand direct access to the memory.

Synchronous DRAM provides the performance to handle these tasks, and as such, moves the memory category to the forefront of overall system performance.



Speed limit 66MHz

While the performance of SDRAM is currently tied to the maximum bus speed of 66MHz, new synchronous technologies provide a path to the future with the advent of Rambus, SynchLink, and SDRAM-II DDR delivering performance of 300MHz and beyond.

Taking the time to plan ahead for this on-going management will be a key factor in making the most of your IT investments. For more details on SDRAM, visit:

www.visiontek.com



Added performance= added complexity

The added complexity of numerous, increasingly sophisticated board-level subsystems all timed on the same clock requires module designers to develop a larger portfolio of systems-specific modules, reducing the overall generic applicability of any given module design. At 100MHz, the problem intensifies, influencing the actual architecture of the modules.

All of these changes boil down to a significantly more complex system configuration puzzle.

Memory management takes on greater importance in the overall picture. As system speeds increase the tolerance between a working module and a disaster waiting to happen narrows, placing a greater burden on the buyer to ensure compatibility with the host system.

Inventory of memory will also become more complex since one module may no longer be suitable for more than one system model in place.

Managing the change

During this evolutionary change in the memory market, it is critical for an enterprise to have an implementation strategy. Knowing which platforms are upgradable, and where they are on the depreciation curve is a fundamental requirement. Correctly linking a platform to a function, and knowing when that system has exceeded its

effectiveness in that function, will provide the opportunity for a planned enhancement and help eliminate roll-out risk. Focused system upgrades and limited subsystem modification will also reduce risk in the lifecycle of your platforms.

The best philosophy is to be consistent in supplier selection and aggressively configure systems to avoid constant interim enhancements. Most importantly, demand quality memory products and suppliers who stand behind their products with a depth of engineering and in-house design resources.

**Get the complete
SDRAM white paper at
www.visiontek.com.**

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